AMENDMENTS IN THE SPECIFICATION

Please remove paragraph number [0006] and replace it with the following rewritten paragraph:

[0006] Also in the CPU 102, but typically not within the processor core 104, is a Level-two (L2) cache 110. Off-board the CPU 102 is a Level-three (L3) cache 112. L2 cache 110 and L3 cache 112, like L1 cache 108, are typically SRAM's. L3 cache 112 is connected, via a system bus 111, to a system memory 113, which is typically a Dynamic Random Access Memory (DRAM), which is slower than SRAM. System memory 113 is connected, via an input/output (I/O) bus [[114]] 124, to a secondary memory 116, which may be a floppy disk drive, a Compact Disk-Read Only Memory (CD-ROM) drive, a Digital Video Disk (DVD) drive, Zip drive, or a hard disk drive storage device.

Please remove paragraph number [0022] and replace it with the following rewritten paragraph:

[0022] Figure 3 is a block diagram of a preferred embodiment of an exemplary disk drive storage device 304 incorporating the present invention. Storage device 304 has a hard magnetic disk 328 as a data record medium, and a magnetic head 322 for reading/writing data from/into the magnetic disk 328. The storage device 304 also has an actuator mechanism 325 for moving a slider which carries the magnetic head 322 to a particular position over a surface of the magnetic disk 328, a voice coil motor (VCM) 324 for causing an access arm of the actuator mechanism 325 to swing, and a VCM driver [[322]] 333 that 1) controls a spindle motor for causing the magnetic disk 328 to rotate and 2) drives the VCM 324. The VCM driver [[322]] 333 includes a 9-bit digital-to-analog converter (DAC), which converts a digital control signal from the MPU 329 into an analog control signal and transmits it to the VCM 324.

Please remove paragraph number [0023] and replace it with the following rewritten paragraph:

[0023] The storage device 304 further has a read/write circuit 326 for controlling a data read/write operation, which contains a module including an amplifier circuit for a detection signal, a waveform shaper, an analog-to-digital converter (ADC), and a digital-to-analog converter (DAC). The storage device 304 also has a hard disk controller (HDC) 337 for controlling the data read/write operation from/into the magnetic disk 328, a microprocessor unit (MPU) 329 for controlling an operation of the entire HDD inclusive of the HDC 337, a ROM 320 for storing microprograms and

data to operate the MPU 329, a Random Access Memory (RAM) 331 for temporarily storing data to be read/written onto the magnetic disk 328 in response to a current read/write request, and an interface (I/F) [[322]] 335 connected to host system 302 through a bidirectional line.

Please remove paragraph number [0024] and replace it with the following rewritten paragraph:

[0024] The HDC 337, the RAM 331 and the MPU 329 are connected to each other through a data bus (not shown). Further, the HDC 337 is connected with the MPU 329 through a control bus (not shown), and is connected with host system 302 through the I/F [[322]] 335.

Please remove paragraph number [0026] and replace it with the following rewritten paragraph:

[0026] Magnetic disk 328 has a plurality of concentric and circular data tracks, each of which includes n LBAs (logical block addresses), where n represents an arbitrary positive integer. The magnetic disk 328 is preferably formatted so as to include a first track having a predetermined number of first sequential LBAs, a second track having a predetermined number of second sequential LBAs which immediately follow the first sequential LBAs, and at least one track disposed between the first track and the second track. The HDC 337, the RAM 331, the MPU 329, the ROM 320 and the I/F [[322]] 335 as a whole constitute a controller [[322]] 339 which controls the operation of the entire disk drive storage device 304 by executing the control program (microprogram) to control read/write requests from host system 302.

AMENDMENTS IN THE DRAWINGS

Please amend Figures 3 and 4a to correct duplicated references numbers, as shown in the attached formal drawings.